UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,102	02/25/2004	Kazuo Asami	009683-499	8810

21839 7590 04/20/2006

BUCHANAN INGERSOLL PC
(INCLUDING BURNS, DOANE, SWECKER & MATHIS)
POST OFFICE BOX 1404
ALEXANDRIA, VA 22313-1404

EXAMINER	
WALTER, CRAIG E	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/785,102	ASAMI ET AL.	
	Examiner	Art Unit	
	Craig E. Walter	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/25/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 25 February 2004 was fully considered by the examiner.

Drawings

3. The drawings were received on 25 February 2004. These drawings are deemed acceptable for examination.

Specification

4. The disclosure is objected to because of the following informalities:

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Appropriate correction is required.

Claim Objections

5. Claim 12-13 are objected to because of the following informalities:

As for claim 12, the phrase "is contained or not" as recited in line 12 of the claim should be changed to "is contained in the table or not" for clarity.

As for claim 13, the phrase "the oldest sector" as recited in lines 6-7 of the claim should be changed to "an oldest sector".

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 9 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Hachiro (JP 07-153284).

As for claim 1, Hachiro teaches a non-volatile memory control device for controlling a non-volatile memory in which data are erased sector by sector and data are written page by page, comprising:

an extracting unit extracting a free page of said non-volatile memory (though a specific unit is not explicitly recited in Hachiro's disclosure, this unit is inherent to his system in order for the system to read (i.e. extract) the physical block (i.e. page), (Fig. 2, element 10) which contains all the necessary

information to determine if a block is free or not based on the extraction. The information provided within the page comprises an elimination flag field; count field of rewriting, and an effective flag field (pages 4, paragraph 0018, all lines). The information contained within this page (along with the erasure and valid flags as described in the abstract) provide information to this system whether the extracted page is free or not);

a first writing unit writing, to the free page extracted by said extracting unit, a directory including a table for translating a logical page number of a page, to which updated data are to be written, to a physical page number (again the unit itself is not explicitly recited in Hachiro's disclosure, however this unit is inherent in order to write the translation table (used to translate the physical page numbers to logical pages numbers) to the free page per Hachiro's teachings recited on page 4, paragraph 0018, all lines); and

a second writing unit writing said updated data to the free page extracted by said extracting unit (the page comprises a location to store updated data (Fig. 2, element 25). Again a unit is inherent in order for the data to be actually written the data area – page 4, lines 0018, all lines).

As for claim 9, Hachiro teaches a non-volatile memory control device according to claim 1, wherein a directory page is set in a fixed page of a plurality of sectors of said non-volatile memory (page 4, paragraph 0018, all lines – the block containing directory information is stored in the non-volatile memory in a fixed location containing a plurality of sectors).

As for claim 11, Hachiro teaches the non-volatile memory control device according to claim 1, wherein said first writing unit successively writes a sixth pointer indicating said table in a fixed sector of said non-volatile memory (Hachiro teaches storing the table at a fixed address. The address (i.e. pointer) must be referenced in order to obtain information from the table; therefore the address of the table itself serves as a pointer to its location).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miller (US Patent 5,638,299) and in further view of Hachiro (JP 07-153284).

As for claim 2, though Miller teaches a data-acquisition system comprising a RAM arranged in a ring and wherein a free page is extracted starting from a lowest page, when a highest page is not a free page (the ring buffer is used to write data to the lowest position once it has determined that the last available storage area (i.e. higest page) has been used (col. 5, lines 12-19)), he fails to teach the remaining limitations of the memory according to claim 1.

Hachiro however teaches a non-volatile memory control device for controlling a non-volatile memory in which data are erased sector by sector and data are written page by page, comprising:

an extracting unit extracting a free page of said non-volatile memory (though a specific unit is not explicitly recited in Hachiro's disclosure, this unit is inherent to his system in order for the system to read (i.e. extract) the physical block (i.e. page), (Fig. 2, element 10) which contains all the necessary information to determine if a block is free or not based on the extraction. The information provided within the page comprises an elimination flag field; count field of rewriting, and an effective flag field (pages 4, paragraph 0018, all lines). The information contained within this page (along with the erasure and valid flags as described in the abstract) provide information to this system whether the extracted page is free);

a first writing unit writing, to the free page extracted by said extracting unit, a directory including a table for translating a logical page number of a page, to which updated data are to be written, to a physical page number (again the unit itself is not explicitly recited in Hachiro's disclosure, however this unit is inherent in order to write the translation table (used to translate the physical page numbers to logical pages numbers) to the free page per Hachiro's teachings recited on page 4, paragraph 0018, all lines); and

a second writing unit writing said updated data to the free page extracted by said extracting unit (the page comprises a location to store updated data (Fig.

2, element 25). Again a unit is inherent in order for the data to be actually written the data area – page 4, lines 0018, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Miller's to further include Hachiro's non-volatile memory into his own data-acquisition system. By doing so, Miller would benefit by having a means of hiding the slow erase process, and reduce the number re-write times of the memory within his system as taught by Hachiro (page ii, lines 25-26).

8. Claims 4-5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hachiro (JP 07-153284) as applied to claim 1 above, and in further view of Guthrie (US PG Publication 2004/0215900 A1)

As for claims 4 and 8, though Hachiro teaches said first writing unit as setting a second flag when writing to a page of data is complete (the valid flag is set to 0 when new data is written as to indicate that the writing of the data is complete (see abstract), he fails to teach a setting a first (or third as per claim 8) flag which indicates that writing to the directory is complete).

Guthrie however teaches a system for reducing contention in a multi-sectored cache in which a vector (i.e. flag) is used to indicate if the writing to a directory entry is complete (paragraph 0046, all lines). Also note, Guthrie teaches the "third flag" as recited by Applicant in claim 8 since the naming of these flags (i.e. first and third) by Applicant is interchangeable, as they both depend directly on claim 1, and have no dependency on one another.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Hachiro to further include Guthrie's method for a multi-sectored cache into his own non-volatile memory. By doing so, Hachiro would benefit by using multiple queues to coordinate overlapping updates, which would help overcome the inefficiencies and system operation degradation that is common to a conventional queue used to store directory entries as taught by Guthrie (paragraph 0013, all lines).

As for claim 5, Hachiro teaches reading the written data, and when the written data matches the read data, rewrites the first flag (again, the valid flag is rewritten after writing the new data to the block (see abstract)).

9. Claims 3, 6-7, 10 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hachiro (JP 07-153284), (as applied to claim 1 for claims 3, 6-7 and 10) and in further view of Holtzhammer (US Patent 5,630,093).

As for claim 12, Hachiro teaches a non-volatile memory control device for controlling a non-volatile memory in which data are erased sector by sector and data are written page by page, comprising:

> a first searching unit searching for a directory page including a table for translating a logical page number of a page, to which updated data are to be written, to a physical page number (referring to the abstract, the system is capable of obtaining data stored at a physical block simply by searching and access the corresponding logical block. The translation table can be stored as part of the page as discussed on page 4, paragraph 0018, all lines),

a second searching unit referring to the table in the directory page searched out by said first searching unit and searching whether a desired logical page is contained or not (information contained within the translation table will indicate the system if a requested logical address corresponds to any physical address. The system can determine that the logical page is not contained within the table if it determines that an entry corresponding to that address is not present (page 4, paragraphs 0018, and 0020 through 0021 all lines)); and

a reading unit reading, when the second searching unit searched out a plurality of desired logical pages, data from a physical page that corresponds to the logical page included in the latest table (data from the page is stored with the translation table in order to allow the system to obtain the data associated with the physical page to be referenced via the logical address (page 4, paragraph 0018, page 4, paragraphs 0018, and 0020 through 0021 all lines)).

Hachiro however fails to teach a first pointer pointing a directory page to be newly written to, and a second pointer pointing a second latest directory page, and successively searching through directory pages based on the first and second pointers included in the directory pages.

Holtzhammer however teaches disk emulation for a non-volatile semiconductor memory utilizing a mapping table which stores directory pages at fixed locations within a non-volatile memory, and further includes linking the page via the use of pointers, as to indicate each successive entry in the chain (see Fig. 10, col. 18, lines 4-29). By using a

linked list of directory entries, Holtzhammer is capable of progressively searching through each of the directory entries.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Hachiro to further include Holtzhammer's non-volatile memory utilizing a mapping table into his own memory. By doing so, Hachiro would benefit by having a means of storing both active and reserve data (i.e. copy), which in turn would provide his system with a redundant copy in order to prevent data loss as taught by Holtzhammer (col. 4, lines 19-28). Holtzhammer specifically teaches how non-volatile memory is prone to failure since it is limited by a finite number of read and erase operations (col. 3, line 63 through col. 4, line 2).

As for claim 13, Hachiro teaches a non-volatile memory control device for controlling a non-volatile memory in which data are erased sector by sector and data are written page by page, comprising:

> an extracting unit referring to a directory page including a table for translating a logical page number of a page, to which updated data are to be written, to a physical page number (referring to the abstract, the system is capable of obtaining data stored at a physical block simply by searching and access the corresponding logical block. The translation table can be stored as part of the page as discussed on page 4, paragraph 0018, all lines)

Hachiro however fails to teach a pointer pointing to the oldest sector and extracting a logical page included in the oldest sector; a searching unit searching

whether a logical page identical with the logical page extracted by the extracting unit is included in any other sector;

Holtzhammer however teaches disk emulation for a non-volatile semiconductor memory utilizing a mapping table which stores directory pages at fixed locations within a non-volatile memory, and further includes linking the page via the use of pointers, as to indicate each successive entry in the chain (see Fig. 10, col. 18, lines 4-29). By traversing the list, Holtzhammer is capable of searching for the oldest sector and determining if it is identical to any other entry within the linked list. The oldest sector can now be erased once an identical entry has been identified.

As for claim 3, though Hachiro teaches all of the elements of claim 1, he fails to teach a said directory including a first pointer indicating a directory page to be newly written next, and a second pointer indicating a second latest directory page. Holtzhammer however teaches disk emulation for a non-volatile semiconductor memory utilizing a mapping table which stores directory pages at fixed locations within a non-volatile memory, and further includes linking the pages via the use of pointers, as to indicate each successive entry in the chain, and where to concatenate the newly written next entry (see Fig. 10, col. 18, lines 4-29).

As for claim 6 and 7, though Hachiro teaches all of the elements of claim 1, he teaches neither a third pointer indicating an oldest sector of a directory, nor a fourth pointer indicating a sector that becomes the oldest when the oldest sector is erased.

Holtzhammer however teaches disk emulation for a non-volatile semiconductor memory utilizing a mapping table which stores directory pages at fixed locations within a

non-volatile memory, and further includes linking the page via the use of pointers, as to indicate each successive entry in the chain, and where to concatenate the newly written next entry (see Fig. 10, col. 18, lines 4-29). Note each successive entry added to the chain indicates a more recent entry, therefore traversing the current list of entries would indicate the age of each successive entry.

As for claim 10, though Hachiro teaches all of the elements of claim 1, he fails to teach the non-volatile memory control device according to claim 1, wherein a fifth pointer indicating a next directory page is stored in a fixed page of a plurality of sectors of said non-volatile memory.

Holtzhammer however teaches disk emulation for a non-volatile semiconductor memory utilizing a mapping table which stores directory pages at fixed locations within a non-volatile memory, and further includes linking the page via the use of pointers, as to indicate each successive entry in the chain (see Fig. 10, col. 18, lines 4-29).

As for claim 14, Hachiro fails to teach a copying unit copying, when said searching unit determines that an identical logical page does not exist in any other sector, said logical page and corresponding directory page to a free page; and said erasing unit erases said oldest sector after copying by said copying unit is complete. (referring to col. 4, lines 6-28, the memory stores an active copy, a redundant copy, and a mapping table to refer to these copies. The clean-up operation as described erases the redundant copy).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Hachiro to further include Holtzhammer's non-volatile memory utilizing a

mapping table into his own memory. By doing so, Hachiro would benefit by having a means of storing both active and reserve data (i.e. copy), which in turn would provide his system with a redundant copy in order to prevent data loss as taught by Holtzhammer (col. 4, lines 19-28). Holtzhammer specifically teaches how non-volatile memory is prone to failure since it is limited by a finite number of read and erase operations (col. 3, line 63 through col. 4, line 2).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Sinclair et al. (US Patent 6,725,321 B1) teach a memory system.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Craig E Walter
Examiner
Art Unit 2188

CEW

9/14/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER